

FIG 1

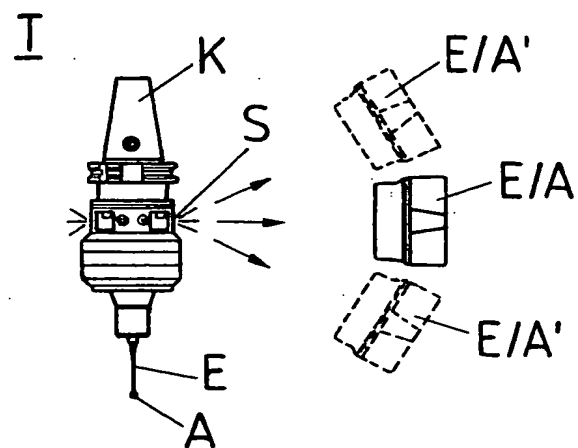


FIG 2

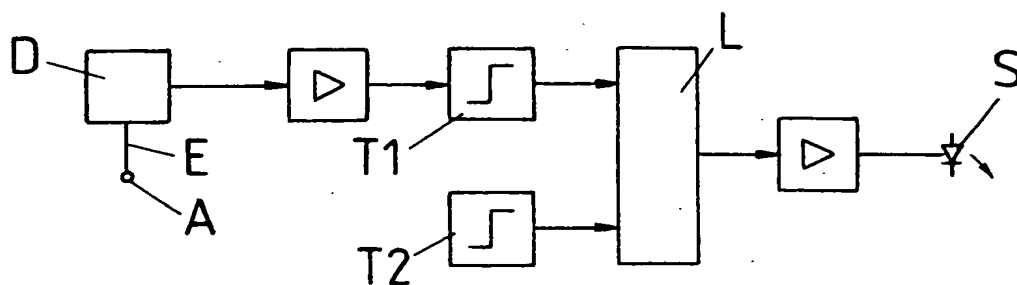


FIG 3A

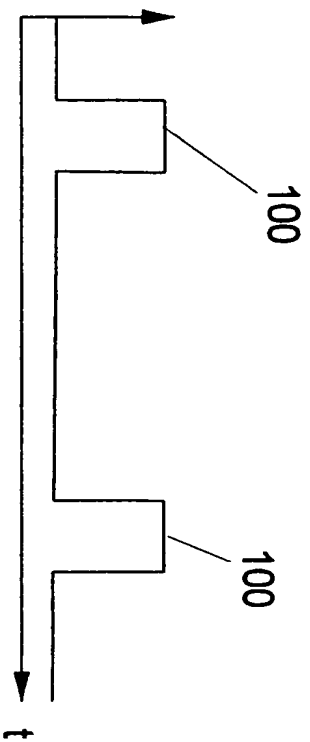


FIG 3B

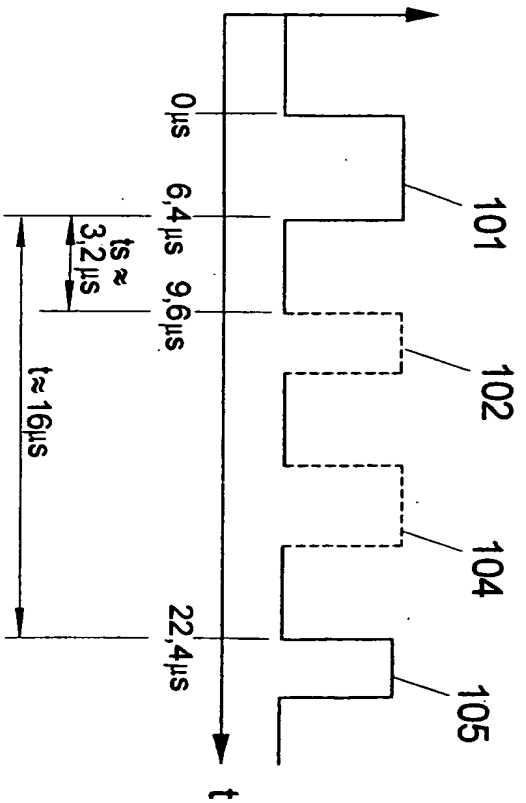


FIG 4

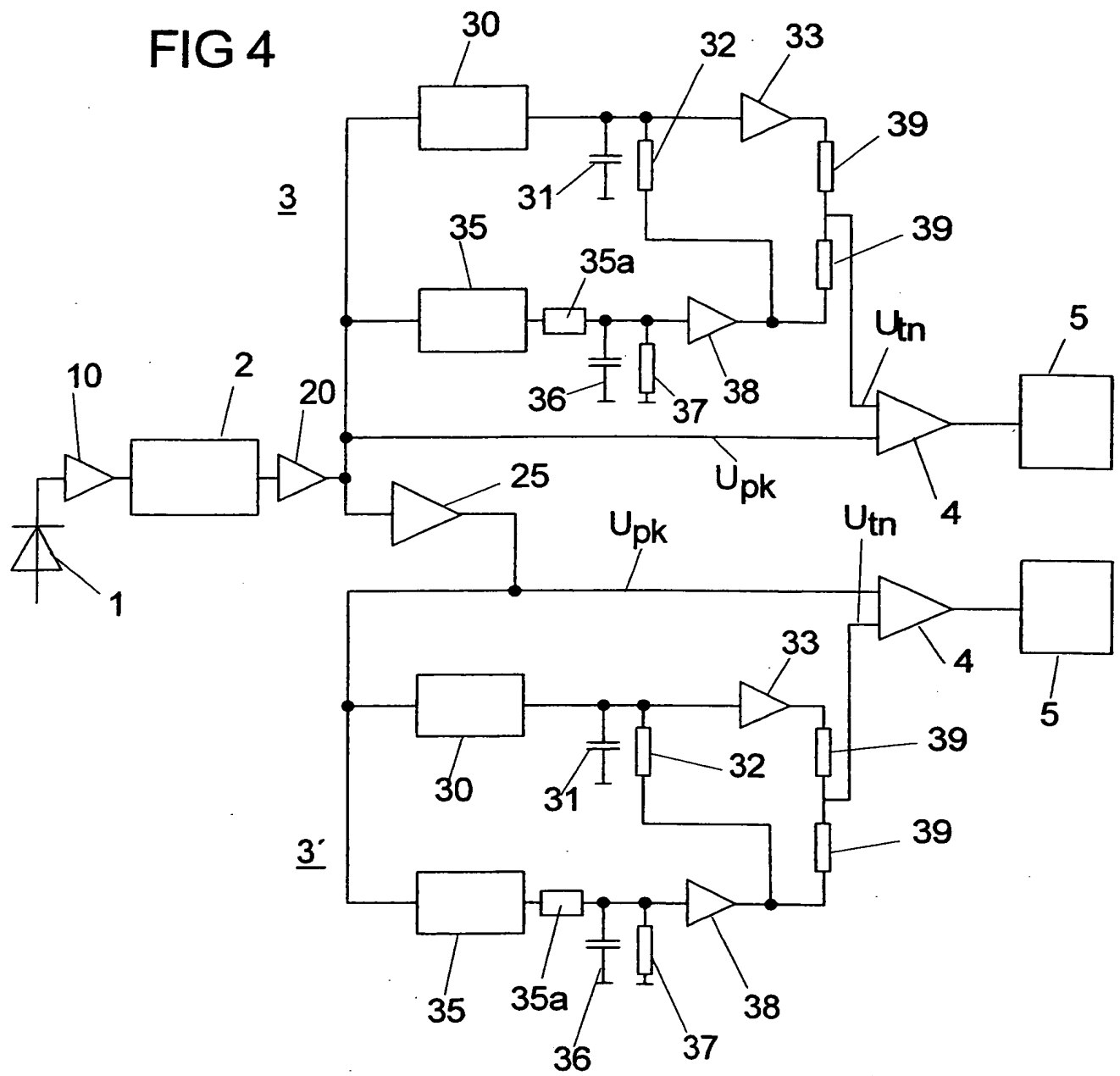


FIG 4A

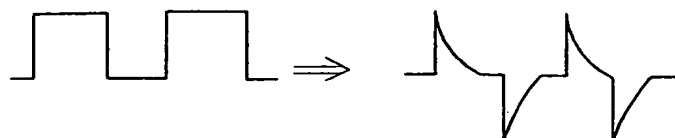


FIG 5

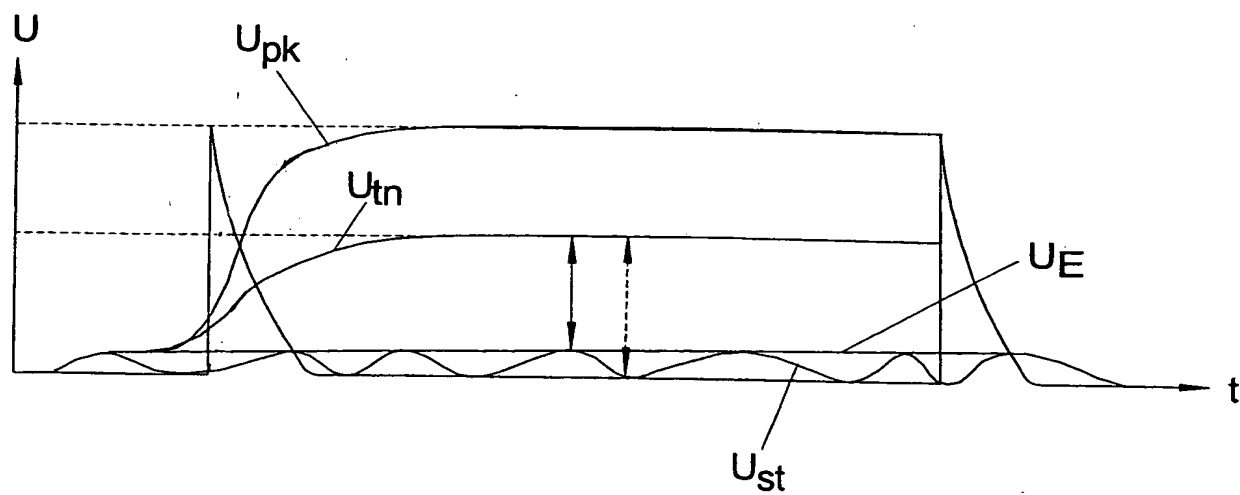


FIG 6A

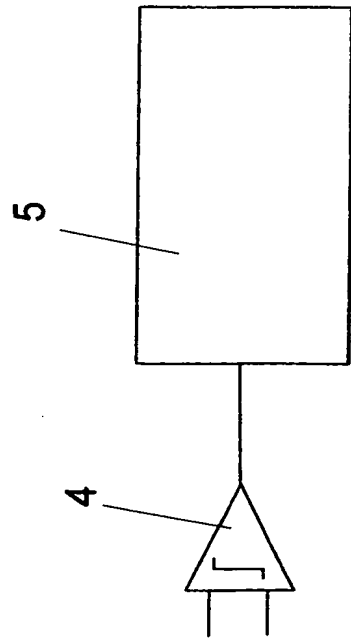


FIG 6B

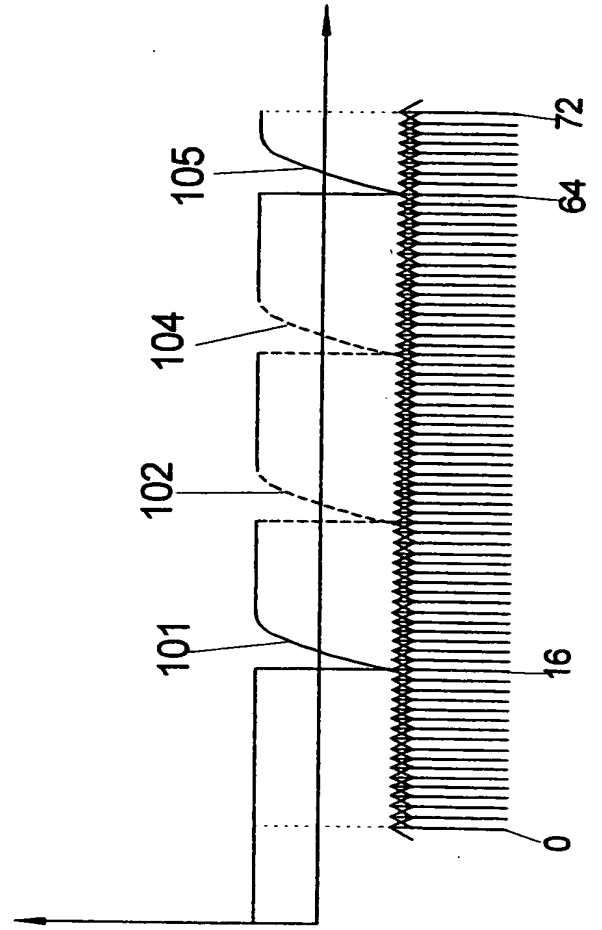
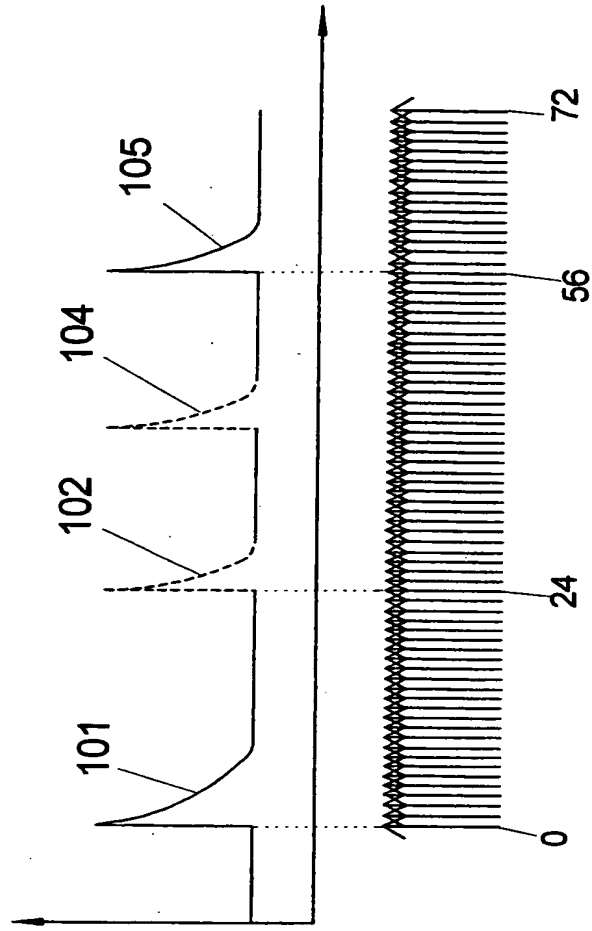


FIG 7

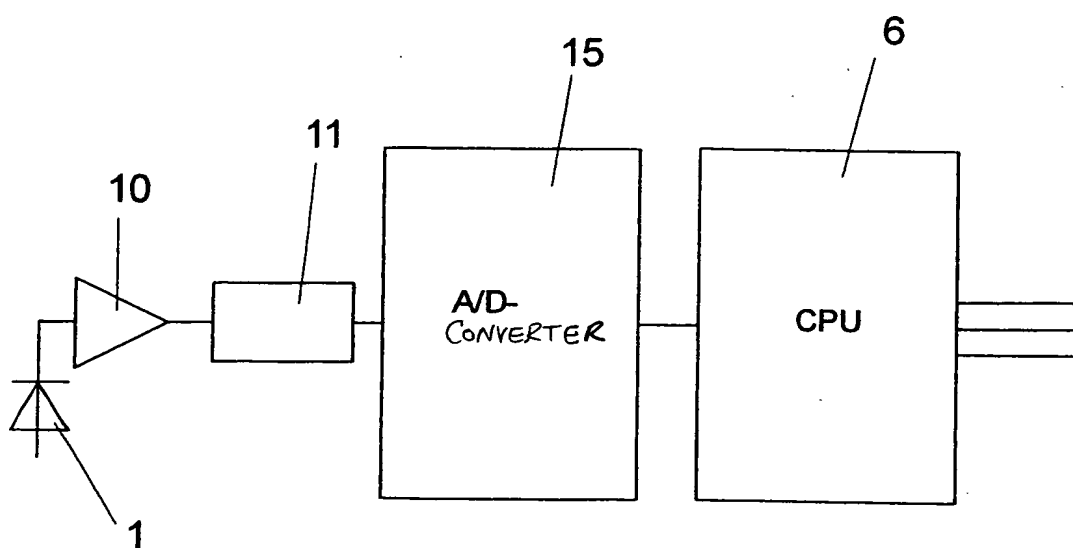


FIG 4

The diagram illustrates a differential signal processing circuit with two parallel channels, labeled 3 and 3'. Channel 3 consists of an input stage with a diode 1 and a buffer 2, followed by a differential pair of transistors 30 and 35. The gates of 30 and 35 are driven by a common-mode input 20 through a buffer 10. The drains of 30 and 35 are connected to a common-mode feedback network consisting of resistors 32 and 37, capacitors 31 and 36, and a current source 35a. The outputs of the differential pair are connected to a differential-to-single-ended converter consisting of a resistor 39 and a buffer 4. The output of channel 3 is labeled 5. Channel 3' is a similar differential pair with transistors 30 and 35, and a common-mode feedback network with resistors 32 and 37, capacitors 31 and 36, and a current source 35a. The output of channel 3' is also labeled 5. The common-mode feedback network is connected to a common-mode input 20 through a buffer 10. The output of the common-mode feedback network is labeled U_{pk} . The output of the differential-to-single-ended converter is labeled U_{tn} .